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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,930	12/15/2005	Yasushi Amamiya	040373-0367	4350

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/560,930	AMAMIYA, YASUSHI	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,9,11,12,14,15,17,20 and 21* is/are rejected.

7)☒ Claim(s) *3-6,8,10,13,16,18,19 and 22-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12-15-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7, 11, 14, 15, 17, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 11, "said differential circuit" on line 4 lacks clear antecedent basis because more than one differential circuit has been recited previously. Further, all the limitations of claim 11 (i.e., bypass path, switching means and control means) appear to be referring to the same components as already set forth in base claim 9. Note also the same problems in claim 14.

As to claim 15, it is not clear if "a clock signal" on lines 9 and 20 is the same as "a clock signal" already set forth on line 5.

As to claim 17, note that it is identical to claim 7 (and that both claims 7 and 17 directly depend from claim 3).

As to claim 20, note that it is identical to claim 18 (and that both claims 18 and 20 directly depend from claim 4).

As to claim 21, note that it is identical to claim 19 (and that both claims 19 and 21 directly depend from claim 5).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, 11, 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Widener (US Patent 4,777,388).

As to claim 1, Widener discloses in figure 2 a current supply control circuit for controlling an amount of current supplied to a differential circuit (16), comprising a bypass path (i.e., conducting path of 28) for bypassing current around said differential circuit; switching means 28, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal C applied from the outside; and control means (the transistor in block 24 directly connected to transistor 42, hereinafter T1) for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal.

As to claim 2, figure 2 of Widener shows the control means T1 for adjusting the amount of current in synchronization with opening/closing of the bypass path (i.e., T1 is ON/OFF when 28 is ON/OFF, respectively).

As to claims 9 and 11, Widener discloses in figure 2 a latch circuit comprising a first differential circuit 16 for reading a data signal D from the outside, a second differential circuit 18 for holding the data signal (i.e., the logic states of the outputs of latch 16 will be held until latch 18 is activated in response to amplifier 20), a first current supply control circuit (see explanation below) for controlling an amount of current supplied to said first differential circuit, and a second current supply control circuit (see explanation below) for controlling the amount of current supplied to said second differential circuit, wherein said first current supply control circuit comprises a first bypass path (i.e., conducting path of 28) for bypassing current around said first differential circuit; first switching means 28, interposed in said first bypass path, for opening/closing said first bypass path in accordance with a signal level of a clock signal /C applied from the outside; and first control means (transistor in block 24 directly connected to transistor 42, hereinafter T1) for controlling the amount of current supplied to said first differential circuit, and said second current supply control circuit comprises a second bypass path (i.e., conducting path of 26) for bypassing current around said second differential circuit; second switching means 26, interposed in said second bypass path, for opening/closing said second bypass path in accordance with a signal level of a clock complementary signal C applied from the outside, said clock complementary signal having a signal level that is the inverse of that of the clock signal; and second control means (the transistor in block 24 directly connected to node B, hereinafter T2) for controlling the amount of current supplied to said second differential

circuit, wherein said first control means adjusts the amount of current in accordance with the signal level of the clock signal, and said second control means adjusts the amount of current in accordance with the signal level of the clock complementary signal.

As to claim 12 and 14, these claims are rejected using the same analysis as applied against claims 9 and 11 above. Note that D and /D are interpreted as a first data signal from the outside, and that the outputs of amplifier 20 are interpreted as a second data signal from the outside.

Allowable Subject Matter

4. Claims 3-6, 8, 10, 13, 16,18, 19 and 22-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 15 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 7, 20 and 21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited in claims. Specifically, none of the prior art teaches or fairly suggests the limitations "said switching means has a current switching transistor, said transistor having an emitter connected to a common emitter of said differential circuit, and said control means is connected to a connection

point between the emitter of said current switching transistor and the common emitter of said differential circuit" as recited in claims 3 and 16; "said control means adjusts the current so that the amount of current supplied to said differential circuit when the signal level of the clock signal is at a low level is larger than the amount of current supplied to said differential circuit when the signal level is at a high level" as recited in claim 6; "said control means adjusts the current so that the amount of current supplied to said differential circuit when the signal level of the clock signal is at a low level is larger than the amount of current supplied to said differential circuit when the signal level is at a high level" as recited in claim 10 and 13; and "said switching means has a current switching transistor, said transistor having an emitter connected to a common emitter of said differential circuit, and said control means is connected to a connection point between the emitter of said current switching transistor and the common emitter of said differential circuit" as recited in claim 15. The remaining claims are allowable due to their dependency upon the claims noted above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on Monday to Friday from 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached at 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

2/14/07